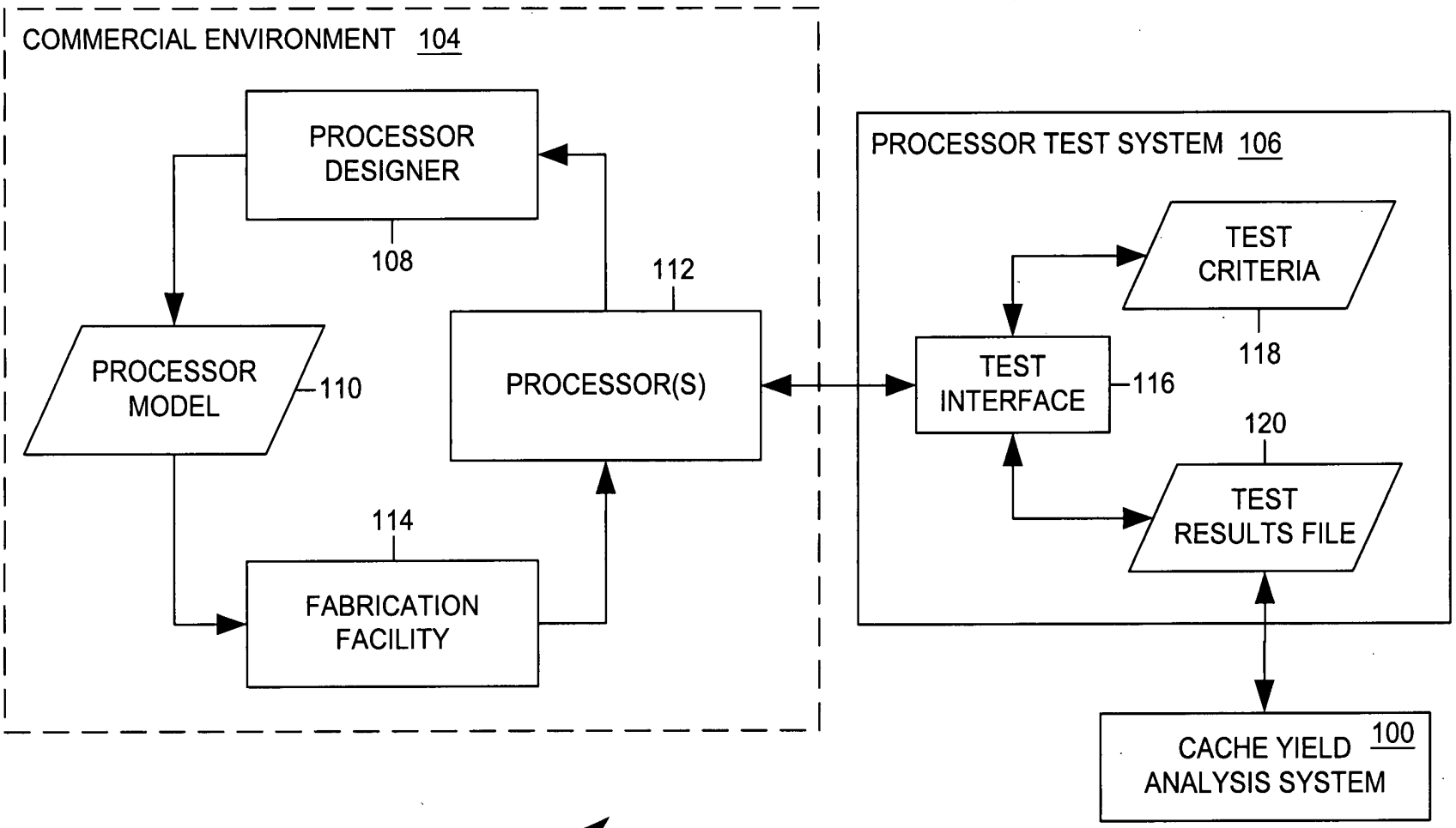
COMMERCIAL ENVIRONMENT 104
PROCESSOR DESIGNER
108
112
PROCESSOR MODEL
110
PROCESSOR(S)
114
FABRICATION FACILITY
PROCESSOR TEST SYSTEM 106
TEST CRITERIA
118
TEST INTERFACE
116
120
TEST RESULTS FILE
CACHE YIELD ANALYSIS SYSTEM
100
102

FIG. 1

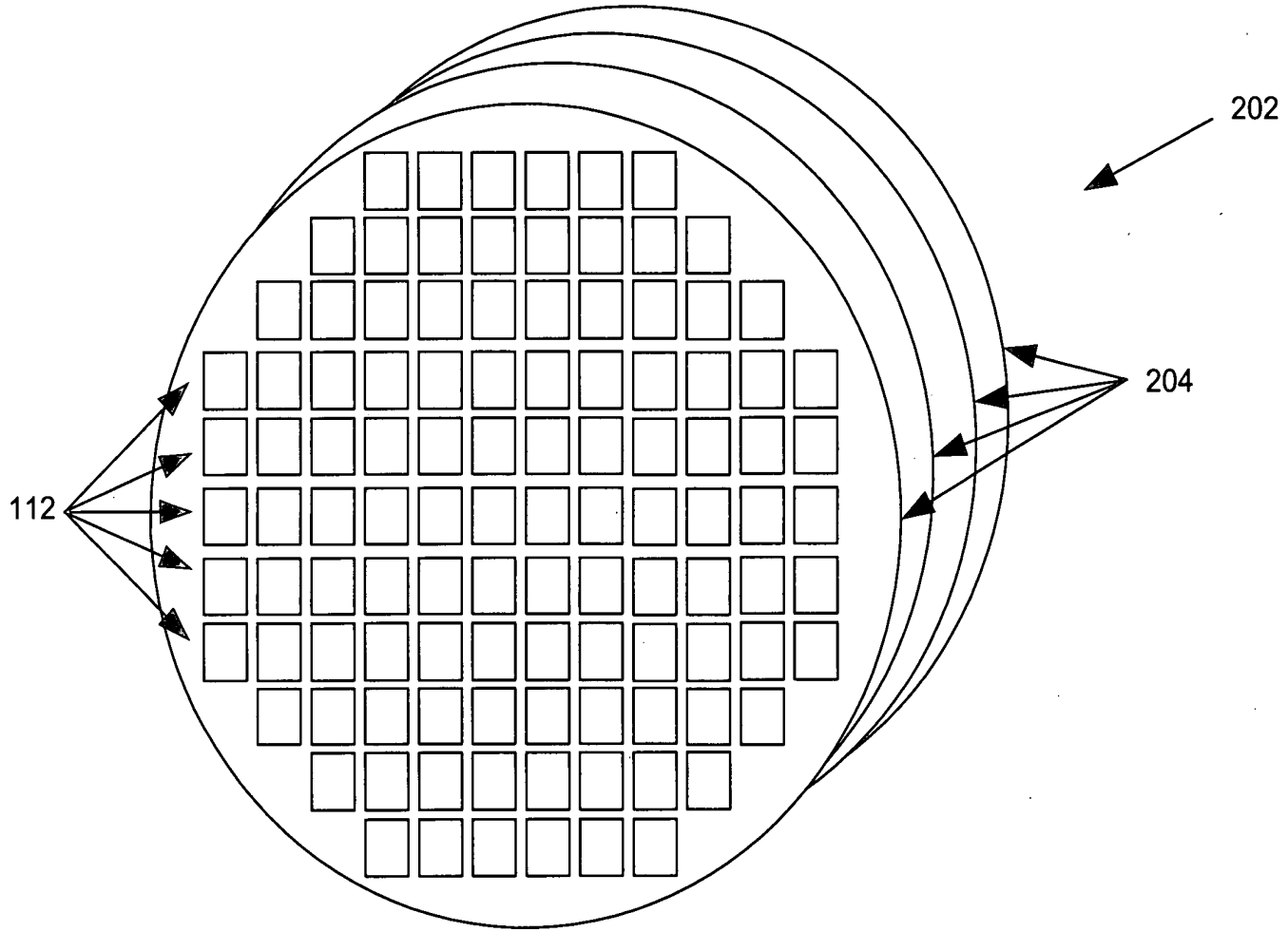

FIG. 2

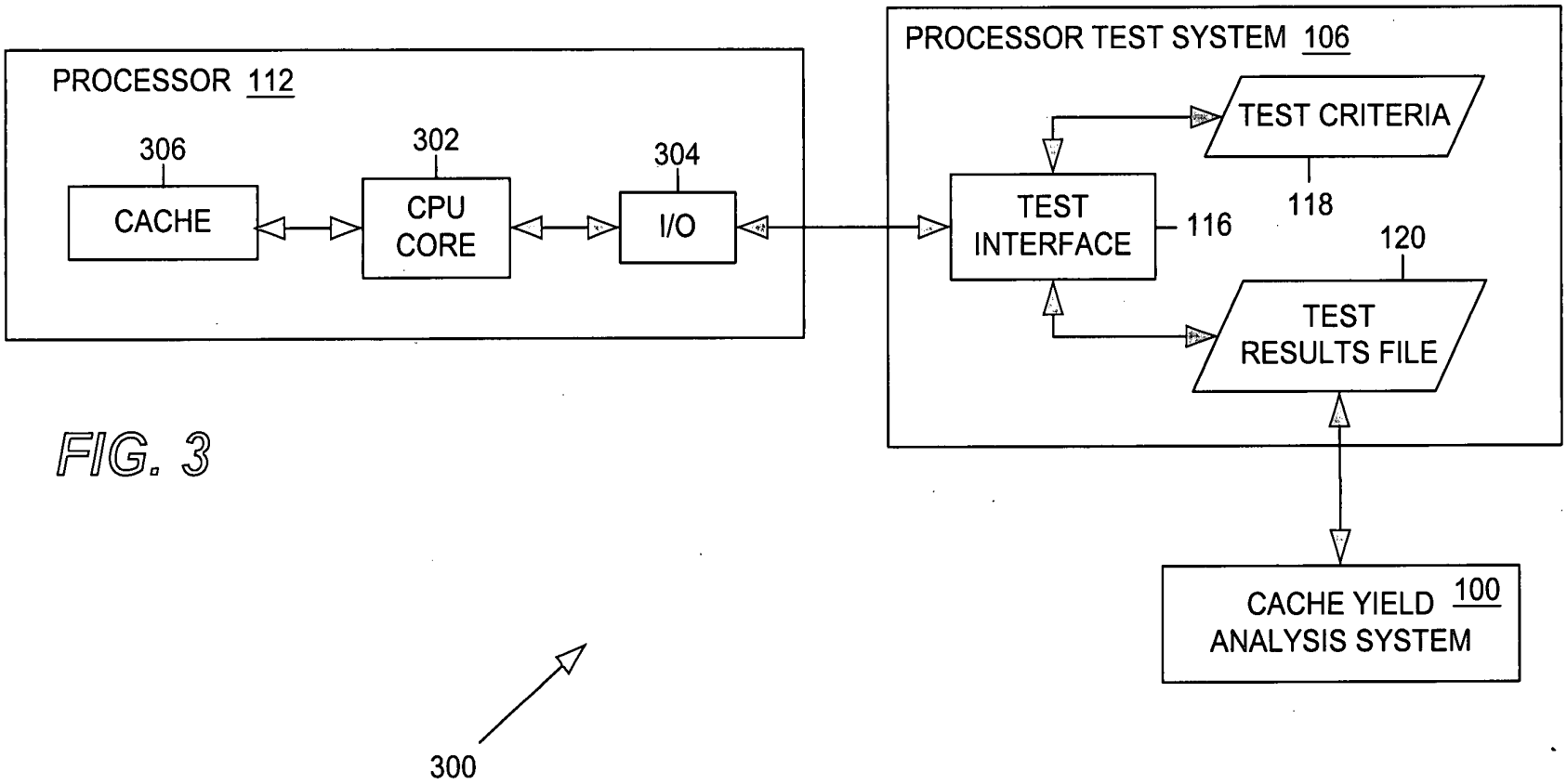
PROCESSOR 112
306
CACHE
302
CPU CORE
304
I/O
PROCESSOR TEST SYSTEM 106
TEST CRITERIA
118
TEST INTERFACE
116
120
TEST RESULTS FILE
CACHE YIELD ANALYSIS SYSTEM 100
300

FIG. 3

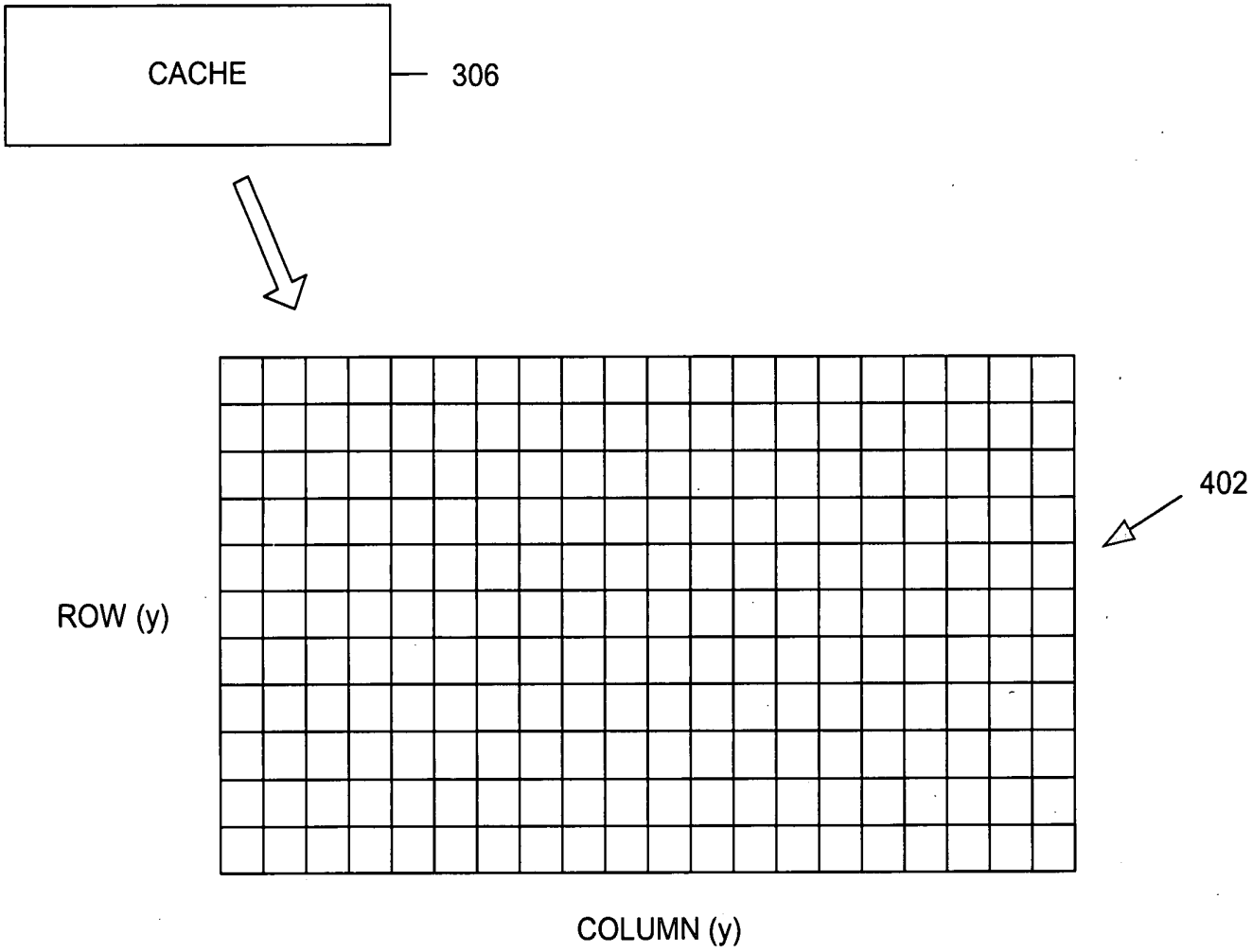

FIG. 4

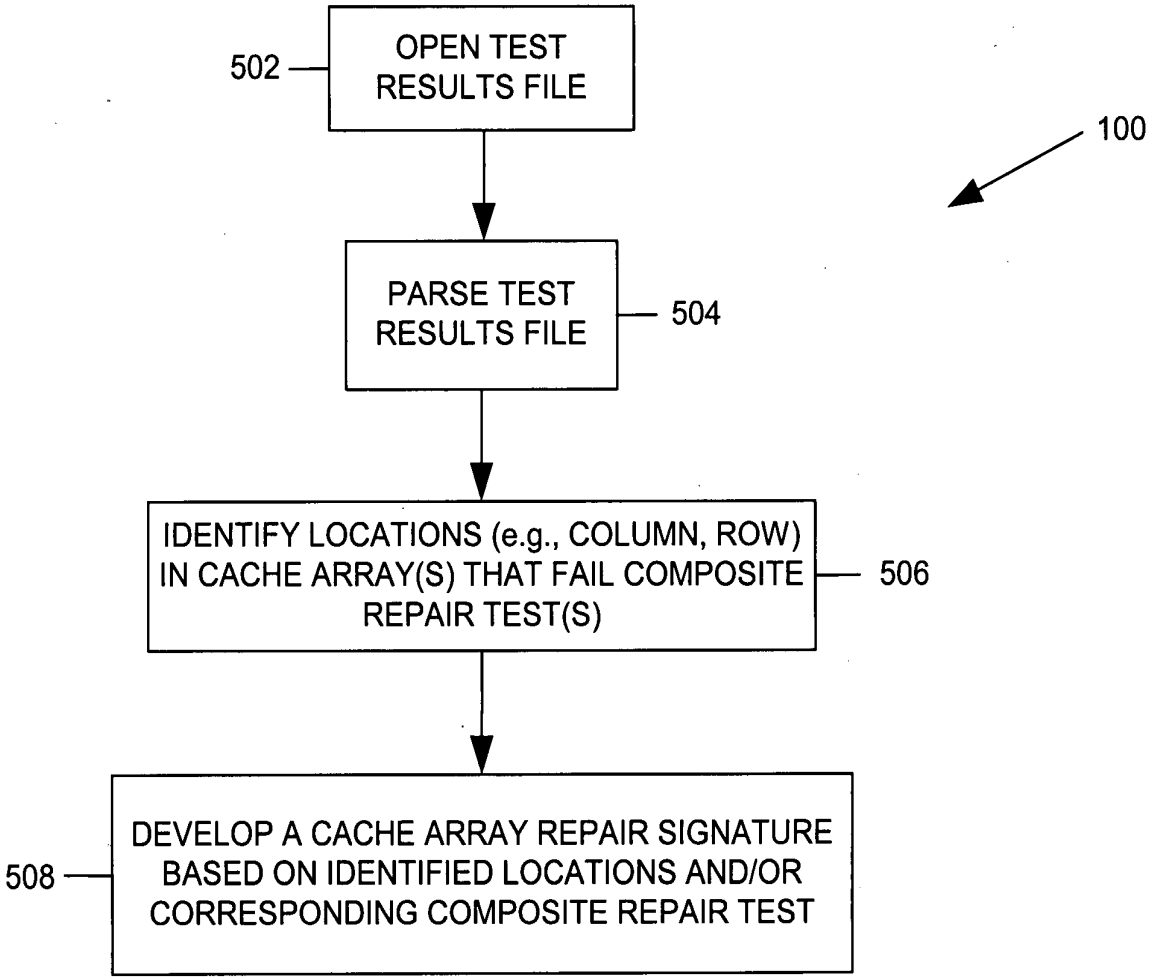
502
OPEN TEST RESULTS FILE
100
PARSE TEST RESULTS FILE
504
IDENTIFY LOCATIONS (e.g., COLUMN, ROW) IN CACHE ARRAY(S) THAT FAIL COMPOSITE REPAIR TEST(S)
506
DEVELOP A CACHE ARRAY REPAIR SIGNATURE BASED ON IDENTIFIED LOCATIONS AND/OR CORRESPONDING COMPOSITE REPAIR TEST
508

FIG. 5

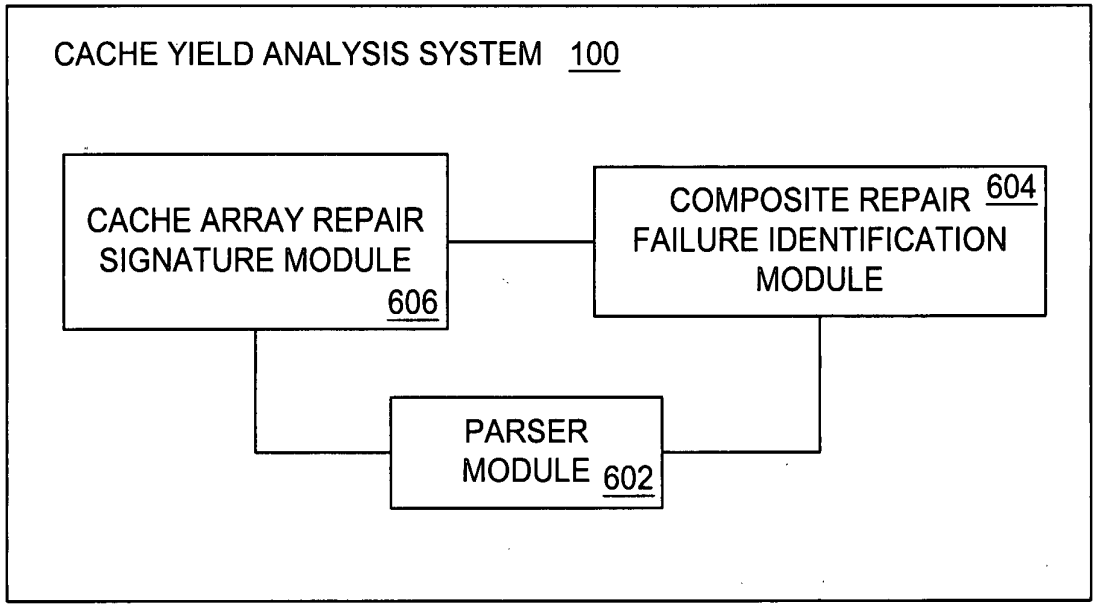
CACHE YIELD ANALYSIS SYSTEM 100
CACHE ARRAY REPAIR SIGNATURE MODULE 606
COMPOSITE REPAIR FAILURE IDENTIFICATION MODULE 604
PARSER MODULE 602

FIG. 6

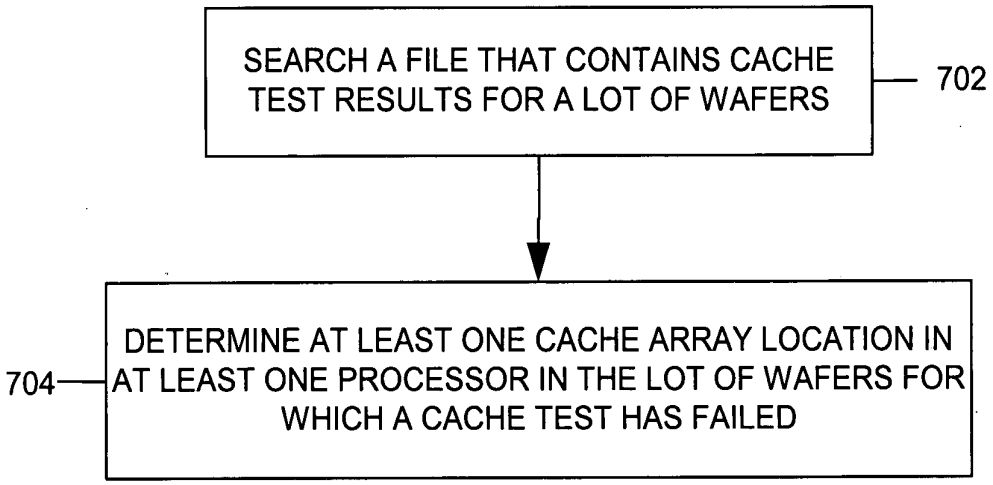
SEARCH A FILE THAT CONTAINS CACHE TEST RESULTS FOR A LOT OF WAFERS
702
DETERMINE AT LEAST ONE CACHE ARRAY LOCATION IN AT LEAST ONE PROCESSOR IN THE LOT OF WAFERS FOR WHICH A CACHE TEST HAS FAILED
704

FIG. 7